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3	PhD Thesis Title	A Novel Architecture- Design of Fongerprint Recognition Process on Filed Programmable Gate Arrays	
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7	Brief synopsis		

7 <u>Brief synopsis</u>

The present works introduce fingerprint recognition process on reconfigurable hardware (FPGA) which is portable, cost effective, faster, reliable, accurate and requires less maintenance. The procedure adapted is as follows: Grey scale image is filtered using parallel architecture to improve the quality of image to lower FAR. The processing time is reduced by adapting fast improved parallel thinning algorithm which is not being handled in earlier FPRS. Proposed thinning algorithm based on IP core not only reduces processing time but also minimizes data size. The proposed work is carried out on three platforms: MatLab, FPGA and ASIC in different stages like pre-processing stage, FPRP and FPRS. Two special hardware methods CORDIC algorithm and IP cores are employed on FPGA to make the proposed work more efficient in terms of processing time, resource utilization, power consumption and recognition rate. Performance evaluation of the proposed work in terms of FAR, FRR, GAR and EER were carried out by considering 100 and 500 samples of individuals between the age of 10 and 65 years. Results with and without preprocessing stage show up 10-15% variations in the recognition rate and with and without post processing, 12-15% variations. Feature extraction without pre-processing and post processing, causes the recognition rate to fall to 70-78%. To analyze the similarity among family members, fingerprint images of 2-G and 3-G family members were considered.